WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

memory cells each of which includes a first MOS transistor having a charge accumulation layer and a control gate formed on the charge accumulation layer with an inter-gate insulating film interposed therebetween; and

a boosting circuit which generates a voltage supplied to the memory cells and includes a capacitor element, the capacitor element including

a first and a second semiconductor layer which are formed on a semiconductor substrate and separated from each other,

a capacitor insulating film which is formed on the top and side of each of the first and second semiconductor layers and on the semiconductor substrate between the first and second semiconductor layers and which is made of the same material as that of the inter-gate insulating film, and

a third semiconductor layer which is formed on the capacitor insulating film and which is connected electrically to the first semiconductor layer and isolated electrically from the second semiconductor layer.

2. The nonvolatile semiconductor memory device according to claim 1, further comprising:

a memory cell array which has the memory cells arranged in matrix and which has columns of the memory cells separated from one another by first element isolating regions; and

word lines each of which is formed by connecting the control gates of the first MOS transistors in the same row in common, wherein

between the first MOS transistors adjacent to one another in the direction of the word line, the charge accumulation layers are separated from one another and the inter-gate insulating film is formed on the top and side of the charge accumulation layer and on the first element isolating region between the charge accumulation layers.

3. The nonvolatile semiconductor memory device according to claim 2, wherein

each of the memory cells further includes a second MOS transistor which has one end of its current path connected to one end of the current path of the first MOS transistor,

the nonvolatile semiconductor memory device further comprises

bit lines each of which connects the other ends of the current paths of the first MOS transistors of the memory cells in the same column in common,

a source line which connects the other ends of the current paths of the second MOS transistors in

common,

select gate lines each of which is formed by connecting the gates of the second MOS transistors of the memory cells in the same row in common,

a column decoder which selects any one of the bit lines,

a first row decoder which selects any one of the word lines, and

a second row decoder which selects any one of the select gate lines, and

the boosting circuit generates a voltage supplied to the first row decoder.

4. The nonvolatile semiconductor memory device according to claim 1, wherein the second semiconductor layer is formed on an element region with an insulating film interposed therebetween, the element region being formed in the semiconductor substrate, the insulating film being made of the same material as that of the gate insulating film of the memory cell.

5. The nonvolatile semiconductor memory device according to claim 1, wherein the second semiconductor layer is formed on a plurality of element regions with an insulating film interposed therebetween, the element regions being formed in the semiconductor substrate and electrically isolated from one another by second element isolating regions, the insulating film being made of the same material as that of the gate

insulating film of the memory cell.

6. The nonvolatile semiconductor memory device according to claim 1, wherein the second semiconductor layer is formed on a third element isolating region formed in the semiconductor substrate.

7. The nonvolatile semiconductor memory device according to claim 1, wherein the dielectric breakdown voltage of a capacitor structure including the charge accumulation layer, the inter-gate insulating film, and the control gate is the same as that of the capacitor element.

8. A nonvolatile semiconductor memory device comprising:

a plurality of memory cells each of which includes a first MOS transistor having a stacked gate including a charge accumulation layer and a control gate formed on the charge accumulation layer with an inter-gate insulating film interposed therebetween;

a memory cell array which has the memory cells arranged in a matrix;

bit lines each of which electrically connects the drain regions of the first MOS transistors of the memory cells in the same column in common;

word lines each of which connects the control gates of the first MOS transistors of the memory cells in the same row in common;

a source line which electrically connects the

source regions of said plurality of memory cells in common;

a column decoder which selects any one of the bit lines;

a first row decoder which selects any one of the word lines; and

a boosting circuit which generates a voltage supplied to the first row decoder and which has a capacitor element including a capacitor insulating film made of the same material as that of the inter-gate insulating film, a part of the capacitor insulating film having the same structure as that of a place where an electric field concentrates most in the inter-gate insulating film.

9. The nonvolatile semiconductor memory device according to claim 8, wherein

the capacitor element includes

a first and a second semiconductor layer which are formed on the semiconductor substrate and separated from each other,

a capacitor insulating film which is formed on the top and side of each of the first and second semiconductor layers and on the semiconductor substrate between the first and second semiconductor layers and which is made of the same material as that of the inter-gate insulating film, and

a third semiconductor layer which is formed

on the capacitor insulating film and which is connected electrically to the first semiconductor layer and isolated electrically from the second semiconductor layer, and

between the first MOS transistors adjacent to one another in the direction of word line, the charge accumulation layers are separated from one another and the inter-gate insulating film is formed on the top and side of each of the charge accumulation layers and on a first element isolating region formed between the charge accumulation layers.

10. The nonvolatile semiconductor memory device according to claim 9, wherein the second semiconductor layer is formed on an element region with an insulating film interposed therebetween, the element region being formed in the semiconductor substrate, the insulating film being made of the same material as that of the gate insulating film of the memory cell.

11. The nonvolatile semiconductor memory device according to claim 10, wherein the second semiconductor layer and the element region are at the same potential.

12. The nonvolatile semiconductor memory device according to claim 9, wherein the second semiconductor layer is formed on a plurality of element regions with an insulating film interposed therebetween, the element regions being formed in the semiconductor substrate and electrically isolated from one another by second

element isolating regions, the insulating film being made of the same material as that of the gate insulating film of the memory cell.

13. The nonvolatile semiconductor memory device according to claim 12, wherein

the second semiconductor layer includes a plurality of fourth semiconductor layers isolated from one another, the fourth semiconductor layers being formed on the plurality of element regions in a one-to-one correspondence with the insulating film interposed therebetween, and

the capacitor insulating film is formed on the top and side of each of the fourth semiconductor layers and on the second element isolating region between the fourth semiconductor layers.

14. The nonvolatile semiconductor memory device according to claim 13, wherein said plurality of fourth semiconductor layers are connected electrically in common.

15. The nonvolatile semiconductor memory device according to claim 9, wherein the second semiconductor layer is formed on a third element isolating region formed in the semiconductor substrate.

16. The nonvolatile semiconductor memory device according to claim 8, wherein

each of the memory cells further includes a second MOS transistor which has a drain region is connected to

the source region of the first MOS transistor, and

the nonvolatile semiconductor memory device further comprises

select gate lines each of which is formed by connecting the gates of the second MOS transistors of the memory cells in the same row in common,

a source line which connects the source regions of the second MOS transistors in common; and

a second row decoder which selects any one of the select gate lines, and

the drain region of the first MOS transistor is connected to the bit line.

17. The nonvolatile semiconductor memory device according to claim 16, wherein the second semiconductor layer is formed on an element region with an insulating film interposed therebetween, the element region being formed in the semiconductor substrate, the insulating film being made of the same material as that of the gate insulating film of the memory cell.

18. The nonvolatile semiconductor memory device according to claim 17, wherein the second semiconductor layer and the element region are at the same potential.

19. The nonvolatile semiconductor memory device according to claim 16, wherein the second semiconductor layer is formed on a plurality of element regions with an insulating film interposed therebetween, the element region being formed in the semiconductor substrate and

electrically isolated from one another by second element isolating regions, the insulating film being made of the same material as that of the gate insulating film of the memory cell.

20. The nonvolatile semiconductor memory device according to claim 19, wherein

the second semiconductor layer includes a plurality of fourth semiconductor layers isolated from one another, the fourth semiconductor layers being formed on said plurality of element regions in a one-to-one correspondence, with the insulating film interposed therebetween, and

the capacitor insulating film is formed on the top and side of each of the fourth semiconductor layers and on the second element isolating region between the fourth semiconductor layers.

21. The nonvolatile semiconductor memory device according to claim 20, wherein the plurality of fourth semiconductor layers are connected electrically in common.

22. The nonvolatile semiconductor memory device according to claim 16, wherein the second semiconductor layer is formed on a third element isolating region formed in the semiconductor substrate.

23. The nonvolatile semiconductor memory device according to claim 8, wherein the dielectric breakdown voltage of a capacitor structure including the charge

accumulation layer, the inter-gate insulating film, and the control gate is the same as that of the capacitor element.